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A novel SOI-MESFET with parallel oxide-metal layers for high voltage and radio frequency applications

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ABSTRACT

In this paper a novel silicon on insulator metal-semiconductor field effect transistor is proposed for high voltage and radio frequency applications. This structure includes additional parallel oxide-metal layers in channel region which we called POML-SOI-MESFET. Our 2-D simulations demonstrate that the presence of parallel layers increases the breakdown voltage. Higher critical electric field of additional oxide region than Si and the effect of inserted metal layer in dispersing the potential lines at the gate edge and also at drift region, boost the breakdown voltage of the device from 13.5 V in conventional structure (C-SOI-MESFET) to 29 V in POML structure which shows 114% improvement. Maximum output power density experiences 133% enhancement by applying POML structure. Also, parallel layers improve the maximum oscillation and cut-off frequencies by 11% and 3.3%, respectively with modifying the gate-drain capacitance. Thermal analysis shows that beside these improvements, the POML maintains the thermal conductivity of the device. In order to attain the best results, POML dimensions are optimized carefully. Simultaneous improvement in breakdown voltage, cut-off frequency, maximum oscillation frequency, and maximum output power density makes our proposed structure an efficient device for applications with higher voltages and frequencies.

1. Introduction

Metal-semiconductor field effect transistors (MESFETs) have attracted much attention in VLSI applications such as commercial optoelectronics, power amplifier for output stage of microwave links, power oscillator, telecommunication, cellular base stations, aerospace, and satellites [1]. These devices beside high electron mobility transistors (HEMTs) [2,3] have been widely considered in RF applications [4–9]. As compared to the MOSFET, the key advantage of the MESFET is the higher mobility of its carriers in the channel. In MESFETs, since the depletion region separates the carriers from the surface, their mobility is more than conventional MOSFETs and is close to that of bulk materials. The higher mobility leads to a higher current, transconductance and transit frequency of the device. The higher transit frequency of the MESFET makes it particularly of interest for microwave circuits [4]. The accomplishment of SOI technology is one of several manufacturing approaches employed to allow the continued miniaturization of microelectronic devices. Some of reported benefits of SOI technology relative to conventional silicon (bulk CMOS) processing which are significant in VLSI applications include: higher performance at equivalent bias, lower leakage current, inherently radiation hardened (resistance to soft errors), and lower parasitic capacitance [5]. The SOI-MESFET is a functional device operating at high power and high speed applications. In addition to RF applications, SOI-MESFETs are appropriate devices in high voltage circuits. They have shown considerably higher breakdown voltages than SOI-MOSFETs [10,11]. But the breakdown for MESFET structures is limited by the gate breakdown as a result of the high electric field at the gate edge beside the drain [12]. There is a tradeoff between the breakdown voltage and the driving current. The large product of channel doping and thickness results in high drain current, which will reduce breakdown voltage.

As stated before, HEMTs are using as high voltage devices beside MESFETs. It is worth mentioning that the breakdown voltage in conventional Si on insulator based MESFETs is about 8–15 V while in conventional HEMT devices this value is very higher. AlGaN/GaN HEMTs on silicon substrates are used as power switching transistors. Compared to silicon power transistors, AlGaN/GaN HEMTs feature low on-state resistances and low switching losses due to the wide bandgap properties. AlGaN/GaN power HEMTs are commercially accessible even in voltage of higher than 1600 V [13]. A group of MESFET devices have used 4H-SiC as channel material [14,15] which shown high breakdown voltages. This group of MESFETs can be compared with HEMT devices

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but the comparison between Si based MESFETs and HEMTs is not sensible in terms of breakdown voltage. These devices have common applications but MESFETs are preferred over HEMTs for applications requiring low phase-noise and temperature insensitive operation [16].

Researchers have reported significant effort for studying and improving the characteristics of MESFET including RF and high voltage specifications [6–9]. A SOI-MESFET structure has been presented with an additional layer of oxide in channel region [12] to supervise the electric field distribution. Simulations have shown that the breakdown voltage improved and drain current experienced a little reduction in comparison with conventional structure. In [9] an SiGe region is used as a well in the buried oxide under the channel region for absorbing the holes generated from impact ionization. Enhancement in breakdown voltage and improvement in self heating effect are the results of HW-SOI-MESFET [9] although the authors have not presented current and frequency analysis. An SOI-MESFET with modified charge distribution has been presented in [6] by insertion of a metal region in the buried oxide of SOI structure. Improvement in breakdown voltage and enhancement in maximum oscillation frequency are the results of applying this modification on SOI-MESFET. Beside the mentioned enhancement, this structure reduces the drain current and cut-off frequency. An SPL-DE SOI-MESFET has been presented [7] which utilizes a p-type layer embedded in drift region and also the doping engineering at source side of channel. The author reported increase in breakdown voltage and improvement in output power density. Increase in drain current and maximum oscillation frequency has also been reported and cut-off frequency has not been investigated. This structure aimed to remove the dependency of the driving current and breakdown voltage on each other [7].

In this paper we propose a novel structure to improve the breakdown voltage, output power density and operating frequencies. This paper aims to get an excellent breakdown voltage beside improvement in RF performance and maximum output power density. The proposed parallel structure includes an oxide region at the right part of the gate metal toward the drain and a metal region at the right lower part of the channel toward the drain region. Dimensions of both regions have been optimized carefully. In POML-SOI MESFET, the additional oxide region due to its higher critical electric field than Si, and metal region due to its ability in dispersion of equi-potential lines in some extent, lead to increase in breakdown voltage of the proposed structure. The extra parallel oxide-metal regions also modify the gate-drain capacitance and consequently improve the operating frequencies.

2. Proposed structure and simulation method

Fig. 1 illustrates the cross-sectional view of the POML-SOI-MESFET.

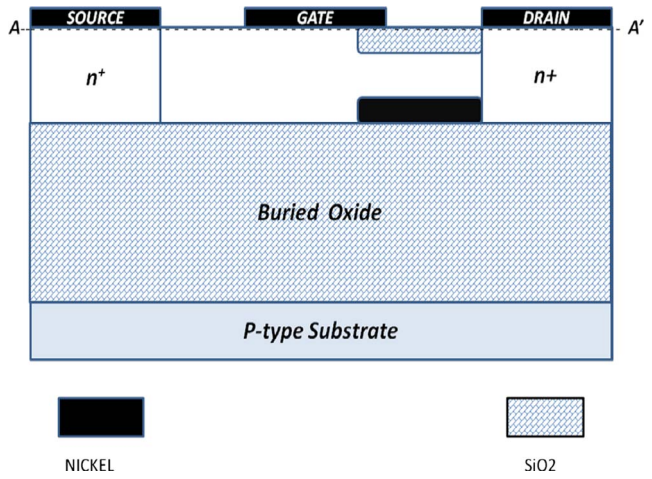

Fig. 1. Schematic cross-sectional view of POML SOI MESFET structure.

Table 1
Utilized parameters for the simulation of the structures.

Parameter	Symbol	Value
Length of source/drain	L_S/L_D	0.3 μm
Length of gate	L_G	0.5 μm
Space between gate and source/drain	L_{GS}/L_{GD}	0.5 μm
Thickness of silicon	T_C	0.2 μm
Thickness of oxide	T_{BOX}	0.4 μm
Thickness of substrate	T_{SUB}	0.1 μm
Doping of source/drain	$N+$	10^{20}
Doping of channel	N	10^{17}
Doping of substrate	P	10^{17}
Width of oxide part	W	30 nm
Width of metal part	W	30 nm
Length of oxide part	L	0.9 μm
Length of metal part	L	0.9 μm
Length of gate	L_G	0.5 μm

Both C-SOI-MESFET and the proposed structures are the same except in additional parallel layers of POML structure. An oxide layer at the top of drift region next to the drain region toward beneath the gate metal and a metal layer at the bottom of channel region next to the drain toward the middle of channel compose the parallel structure. The related and required parameters for simulations have been mentioned in Table 1. The parallel layers dimensions have been extracted after carefully optimization of parameters which will be discussed in the last part of paper. Atlas simulator from SILVACO [17] has been used for 2-D simulations. The required models have been activated to get reliable outputs from simulator. In addition to basic Poisson and drift diffusion equations, other models such as CONMOB, FLDMOB, ANALYTIC, BBT.STD, AUGER, SRH, IMPACT SELB, INCOMPLETE, and LAT TEMP have been activated too, for considering physical phenomena responsible for breakdown and determination of RF characteristics of the device. It is important to calibrate the simulator with experimental data. Fig. 2 shows the results of comparison between the experimental data [18] and simulator outputs. A good agreement between them is apparent.

3. Proposed fabrication process flow

We offer a process flow for the fabrication of the POML-SOI MESFET in Fig. 3, which employ the normal techniques for the formation of the SOI device. The initial materials are an n-type ⟨1 0 0⟩ oriented silicon wafer called “wafer A” and one p-type ⟨1 0 0⟩ oriented silicon wafer named “wafer B”, which have been illustrated in Fig. 3a. Via definition is done in Fig. 3b. Depositing a layer of oxide on the wafer A is the next

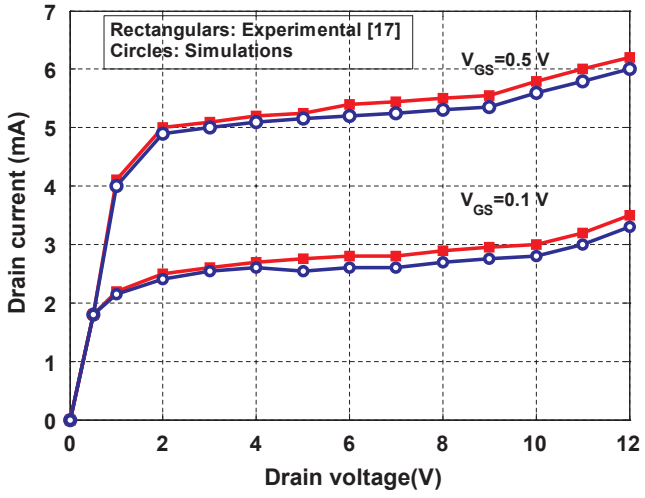

Fig. 2. Comparison between simulation results and experimental data [18].

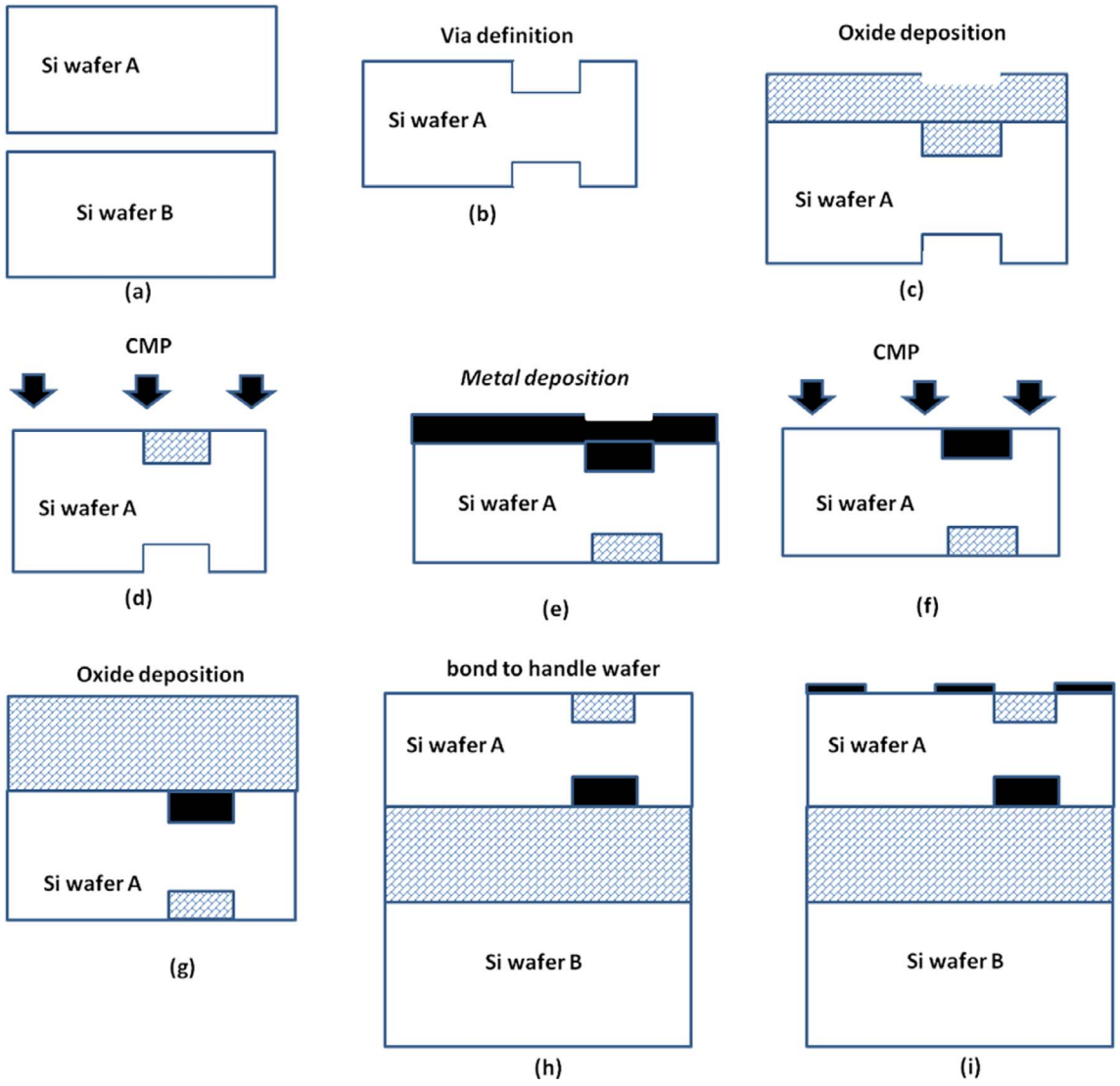

Fig. 3. The proposed fabrication process for POML structure.

step as shown in Fig. 3c. Fig. 3d shows that a treatment such as CMP can be executed to eliminate the uneven surface left after oxide deposition. After removing additional oxide, in another side of wafer A, a layer of metal is deposited on the silicon (Fig. 3e). Fig. 3f shows that again a treatment such as CMP can be performed to eliminate rough surface left after metal deposition. Oxide deposition can be done on the wafer A (Fig. 3 g). Fig. 3 h shows wafer B which is bonded to support wafer A by wafer bonding. Finally, a straight fabrication process will be employed to complete the fabrication in Fig. 3i. From above process it can be seen that some additional steps are required due to the development of additional layers which is approximately a common feature for novel structures. These steps are known processing stages and similar to those steps which are employed by conventional fabrication process [6,7,9,12,14].

4. Simulation results

Output characteristics of C-SOI-MESFET and POML-SOI-MESFET structures have been illustrated in Fig. 4 at different gate source voltages. By applying the parallel structure a minor reduction in device current capability is seen. This reduction is due to the decrease in effective channel thickness of the POML structure by inserting the parallel layers. It is observed that this reduction is trivial and doesn't have

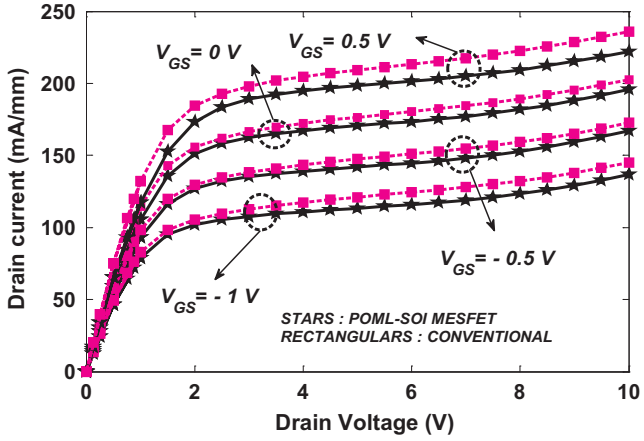

Fig. 4. Output characteristics of the proposed and conventional structures at different gate-source voltages.

significant effect on the device performance at high voltage applications.

To evaluate the breakdown voltage of both structures, the drain current as function of the drain voltage is shown in Fig. 5 at bias

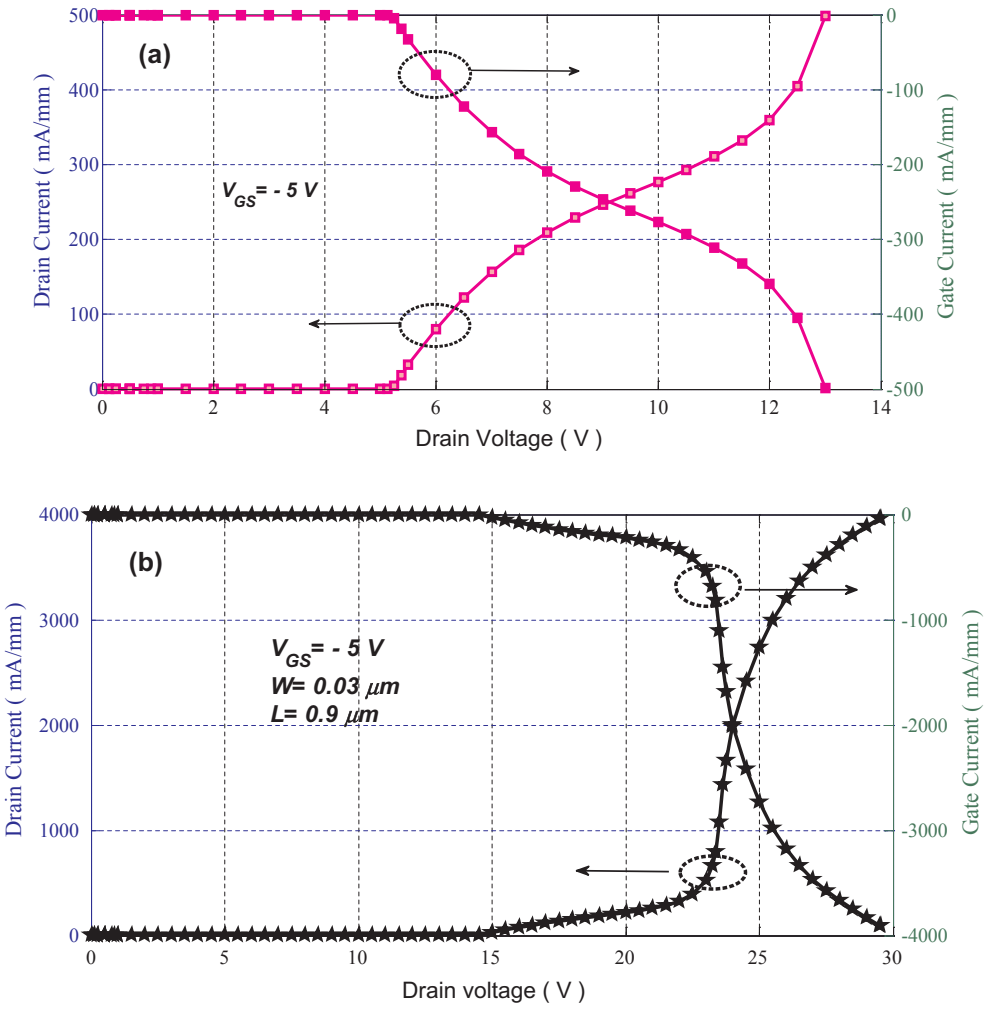

Fig. 5. Three-terminal breakdown characteristics of (a) C-SOI-MESFET and (b) POML-SOI-MESFET.

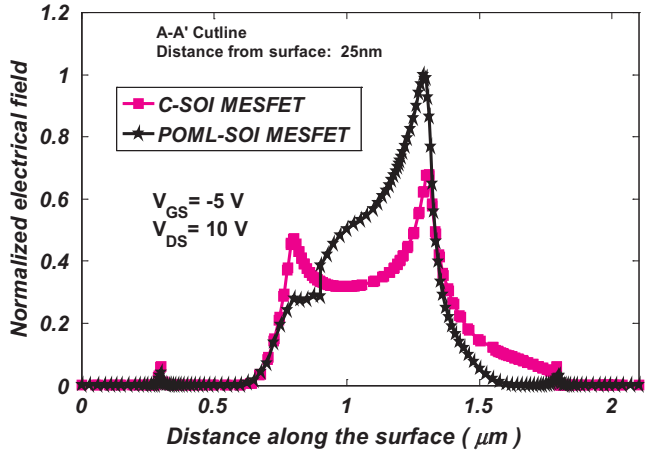

Fig. 6. Electric field distribution along the surface at bias V_{DS} = 10 V, V_{GS} = −5 V and A-A′ cutline for 25 nm distance from surface.

V_{GS} = −5V for C-SOI and POML-SOI structures. C-SOI breakdown voltage occurs at 13.5 V, whereas in POML-SOI reaches 29 V and shows more than 114% enhancement. This progress is related to the role of parallel layers. The Breakdown voltage is determined by distribution of equi-potential lines and critical electric field of the material. Fig. 6, illustrates the normalized electric field distribution along the surface at A-A' cutline (25 nm distance from surface) and bias V_{DS} = 10 V and V_{GS} equal to the threshold voltage ∼ −5 V. The oxide part is located at drain side of gate metal where the electric field reaches its maximum value. Breakdown voltage happens where maximum electric field reaches the material critical field. Critical electric field is the maximum magnitude of electric fields which the material can tolerate without breaking down. The maximum electric field occurs at drain side, at the gate metal corner of conventional MESFET. In this region, we used oxide instead of Si. The critical field of oxide is considerably higher than Si. Thus, oxide can tolerate higher fields and voltages. The critical electric field of Si, and SiO_2 are ∼0.3 and ∼10 MV/cm respectively which shows about 300 times higher tolerable field in latter material [19,20]. Substitution of Si with SiO_2, in turn, increases the electric field inside the material. As can be observed in Fig. 6, which shows the electric field distribution along the surface for both structures, the magnitude of maximum electric field in SiO_2 is about 40% higher than Si, but due to the very high critical field of oxide, POML structure not only tolerate this field but also can tolerate much higher values.

As Fig. 7 shows, existence of oxide region inherently makes potential lines closer under the gate metal at drain side and increases the electric field in comparison with its C-SOI-MESFET counterpart but its larger critical field can tolerate this field and improves the breakdown voltage. In addition, the metal layer at lower part of parallel configuration helps more effective management of electric field. Inserting metal layer scatters potential lines, not completely but to some extent and helps reduction in potential derivation and consequently more increment in breakdown voltage. These two factors are responsible for breakdown voltage enhancement in POML structure.

The theoretical maximum output power density (P_{max}) of class A amplifier is calculated as follow [21]:

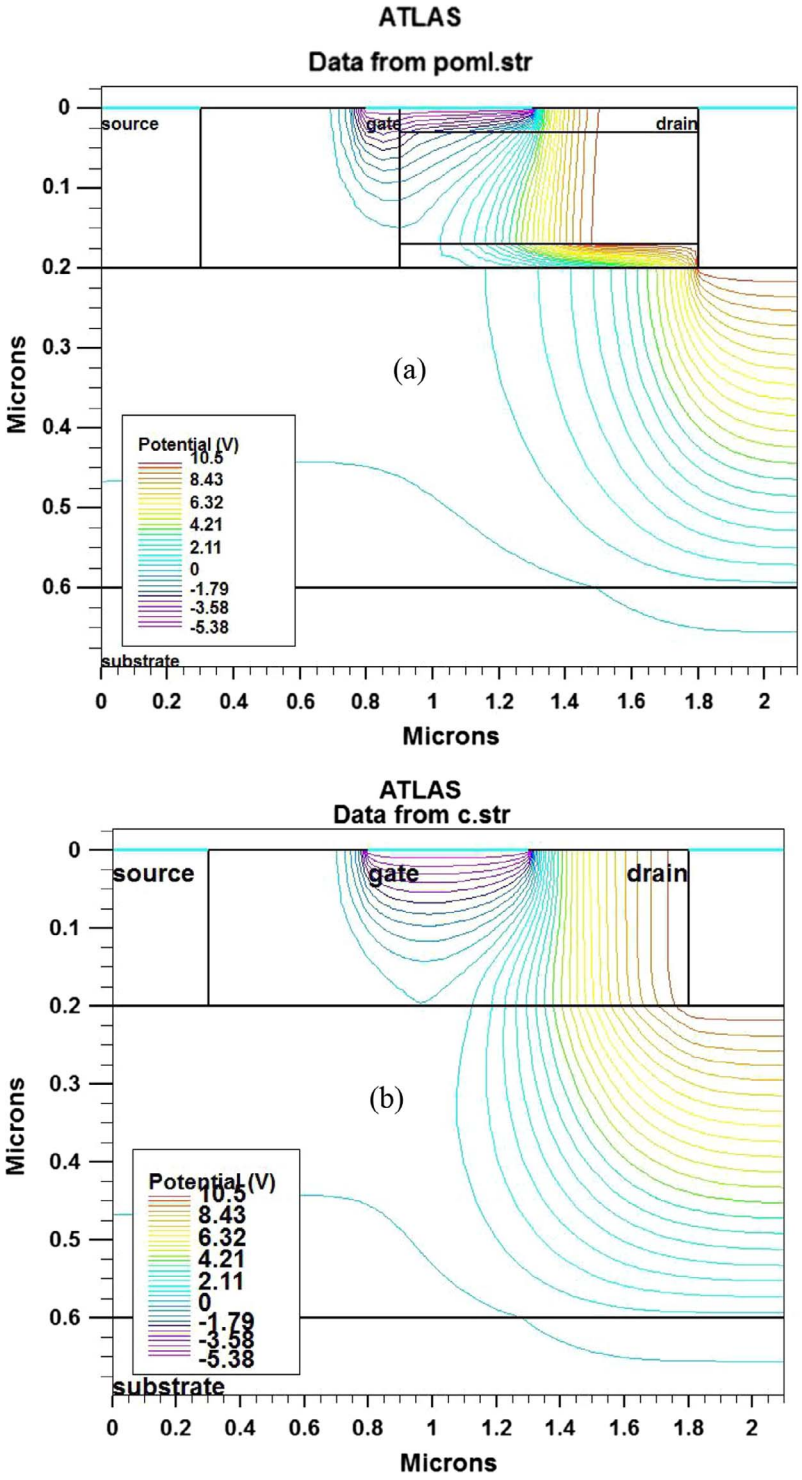

Fig. 7. Simulated equi-potential contours at $V_{DS} = 10\,V$, $V_{GS} = -5\,V$ for the (a) POML-SOI-MESFET and (b) C-SOI-MESFET.

$$P_{max} = \frac{I_{DSAT}(V_{BR} - V_{Knee})}{8} \quad (1)$$

where V_{BR} is breakdown voltage, V_{Knee} is the knee voltage, and I_{DSAT} is saturation current. As can be observed from above equation, P_{max} value depends on bias conditions because all its three elements varies with bias conditions. In this study, the bias conditions applied to the structures are set to be $V_D = 10$ and $V_G = -5\,V$. Mainly, due to the higher breakdown voltage we expect that P_{max} is improved in POML structure. Calculations demonstrates that P_{max} of our proposed structure is 0.513 W/mm which shows 133% improvement in comparison with its conventional structure with $P_{max} = 0.22$ W/mm. From above simulations and the obtained results one can conclude that regarding to the excellent P_{max} and superior V_{BR}, the POML structure is a better-quality structure than its conventional counterpart in terms of DC characteristics for high voltage applications.

In spite of all the advantages of the SOI over the bulk technology, the self-heating effect is a severe issue troubling the device performance due to lower thermal conductivity of the buried oxide as compared to the silicon. In most cases, modification in device structure causes to damage the thermal conductivity of the device. A proper structure, beside improvement in DC and RF performance, should enhance the thermal behavior of the device or at least maintains its thermal

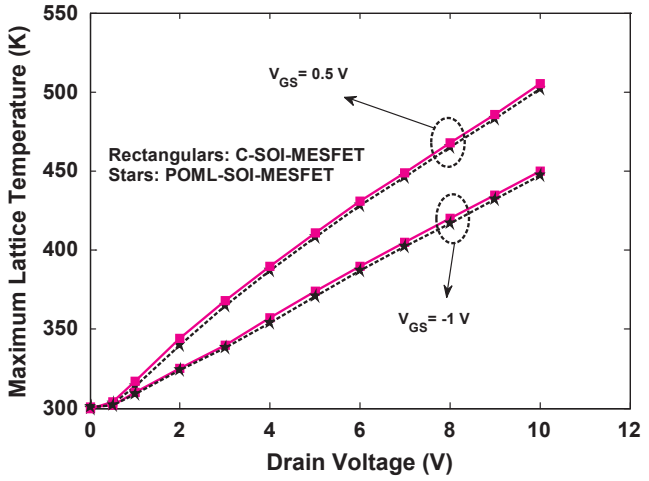

Fig. 8. Maximum lattice temperature versus drain voltage at $V_{GS} = -1$ and 0.5 V for conventional and POML-SOI structures.

conductivity. Thus it is important to investigate the lattice temperature for POML and compare it with conventional structure. The maximum lattice temperature versus the drain voltage for the POML and the conventional structure is extracted at the biases $V_G = -1$ and 0.5 V as shown in Fig. 8. It is worth noting that the substrate contact temperature is fixed at 300 K. It can be seen that both structures have similar maximum lattice temperatures. POML structure causes to small reduction in maximum temperature. The additional parallel layers act in opposite direction to increase or decrease the maximum lattice temperature. The oxide layer decreases the channel thickness and increases the lattice temperature. The metal layer due to its higher thermal conductivity acts as a factor to decrease the lattice temperature. Our simulations show that these two factors approximately neutralized each other and only a little decrease in lattice temperature is observed which is desirable. This shows that by applying the POML structure, the DC and RF characteristics are improved while the proposed structure doesn't have destructive effects on device thermal conductivity.

Presence of metal and oxide parallel layers influences RF parameters in addition to DC characteristics. To investigate this issue, we studied current gain (h_{21}), and unilateral power gain (UPG). Maximum oscillation frequency (f_{max}) is extracted from UPG graph and cut-off frequency (f_T) is obtained from current gain graph where they get 0 dB values. Simulations confirm that POML structure increases both f_T and f_{max} in comparison with conventional structure. Results have been illustrated in Fig. 9. It is seen that POML structure increases f_T from 17.7 to 18.3 GHz and f_{max} from 83.5 to 92.5 GHz. These frequencies have been extracted in biasing $V_G = 0$ V and $V_{DS} = 10$ V. To investigate the reason for these results, one can refer to below equations [21–23]:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2}$$

$$f_{\max} = \frac{f_T}{2}\sqrt{\frac{R_{DS}}{R_G}} \tag{3}$$

where C_{GS} is gate-source capacitance, C_{GD} is gate-drain capacitance, R_{DS} is the drain–source resistance, R_G is the gate resistance, and g_m is transconductance. Fig. 10 illustrates transconductance versus gate source voltage at frequency of 10 GHz. It can be seen that POML transconductance is lower than C-SOI. Gate drain capacitance is a critical variable in high frequency applications showing the output signal feedback to the input. This parameter actually shows the coupling between the gate and drain. Fig. 11 illustrates the gate drain capacitance at different biases and frequency 10 GHz. It can be observed that our proposed structure has lower capacitance for all of investigated biases. The main reason for this improvement is attributed firstly to the

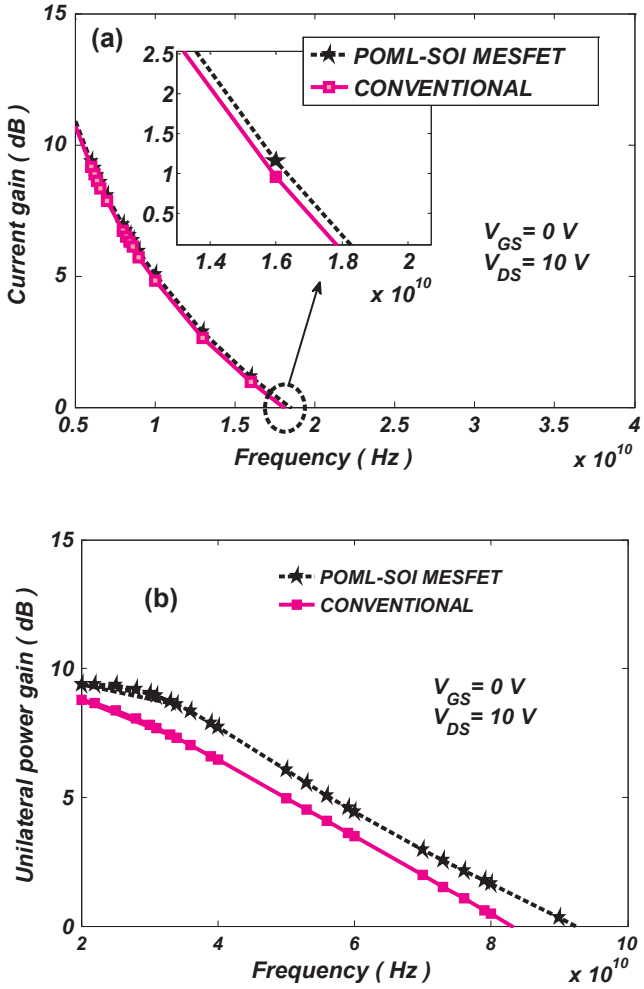

Fig. 9. (a) Current gain and (b) Unilateral current gain versus frequency for C-SOI MESFET and POML-SOI MESFET.

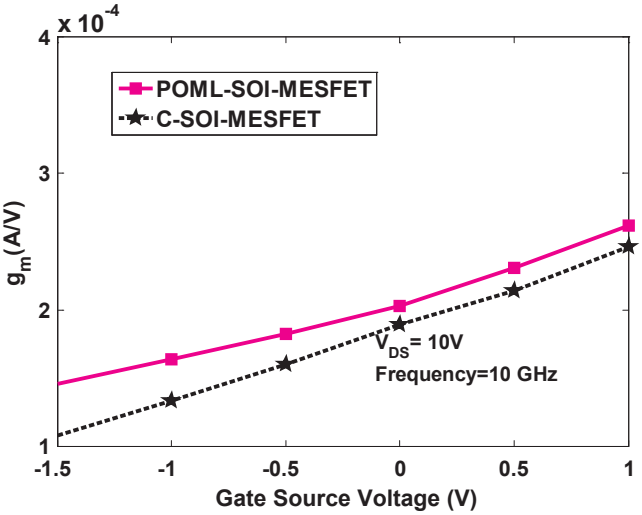

Fig. 10. Transconductance at different gate-source voltages for C-SOI MESFET and POML-SOI MESFET.

function of additional oxide layer on drift region and secondly to the creation of a new capacitance due to the presence of additional metal layer. Additional oxide layer operates as a practical blockage in extending the depletion region underneath the gate into the drift region

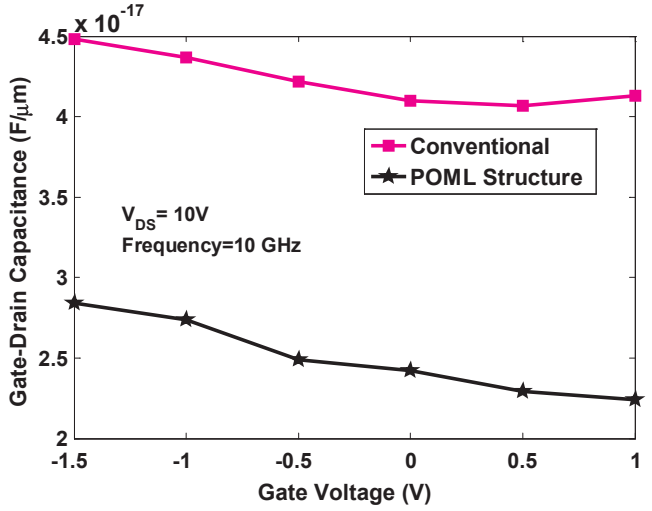

Fig. 11. Gate-Drain capacitance at different gate-source voltages for C-SOI MESFET and POML-SOI MESFET.

and lowers the coupling between output and input. Also, the additional metal region capacitance is in series with C_{GD} leads to lower total capacitance between gate and drain. It is seen that g_m and gate capacitance move in opposite direction to increase or decrease cut-off frequency, respectively but simulations show that the effect of gate capacitance is stronger than that of g_m and cut-off frequency increases. Eq. (3) shows that maximum oscillation frequency depends on two factors; cut-off frequency f_T and R_{DS}/R_G ratio. As we stated before, POML current shows a trivial reduction which means a little increase in its drain-source resistance and consequently higher R_{DS}/R_G ratio. So, f_T and this ratio move in same directions and consequently f_{max} increases.

Tables 2–5 present the comparison between POML and some of recently reported SOI-MESFET structures. The main device characteristics including breakdown voltage, current capability, f_t, and f_{max} depend on device physical dimensions (the length of gate, drain, source, and so on), doping density, bias conditions, and activated models in SILVACO software. Recently reported novel SOI-MESFET have been simulated in different conditions and parameters so that they are not directly comparable. To compare POML with other structures at fair conditions, we simulate POML again with parameters equal to those which have been used in simulation of previously reported structures. It means that POML and each recently proposed structure are compared one by one. It can be seen that POML outperforms other structures.

5. Optimization of parallel layers dimensions

Our simulations reveal that parallel oxide and metal layers have desirable effects on DC and RF performance of SOI-MESFEs. Therefore, study of the dimensions of these layers is necessary to obtain the more optimized results. Based on 2-D simulation, by optimization of layer dimensions a high performance of the POML-SOI-MESFET can be achieved. The length and width of both layers have been changed accordingly. We assume equal length for both layers and also equal width for them. Fig. 12 presents the results of variations in parallel layers length where the oxide and metal widths are fixed at 30 nano meter.

Table 2
Comparison between MR [6] and our proposed structure with the dimensions, bias conditions, and device parameters which have been used in [6].

Structure	Breakdown voltage	Current $V_{GS}=0$ V, $V_{DS}=5$ V	f_{max}	f_t
MR [6]	20.5 V	100 mA/mm	98 GHz	25 GHz
POML	29 V	110 mA/mm	99 GHz	24.5 GHz

Table 3
Comparison between DPG [24] and our proposed structure with the dimensions, bias conditions, and device parameters which have been used in [24].

Structure	Breakdown voltage	Current $V_{GS}=0$ V, $V_{DS}=5$ V	f_{max}	f_t
DPG [24]	19 V	Not reported	70 GHz	25 GHz
POML	28 V	140 mA/mm	91 GHz	24.5 GHz

Table 4
Comparison between SPL-DE [7] and our proposed structure with the dimensions, bias conditions, and device parameters which have been used in [7].

Structure	Breakdown voltage	Current $V_{GS}=0$ V, $V_{DS}=5$ V	f_{max}	f_t
SPL-DE [7]	14 V	150 mA/mm	75 GHz	Not reported
POML	28.5 V	135 mA/mm	86 GHz	22 GHz

Table 5
Comparison between T-SOP [22] and our proposed structure with the dimensions, bias conditions, and device parameters which have been used in [22].

Structure	Breakdown voltage	Current $V_{GS}=0.5$ V, $V_{DS}=5$ V	f_{max}	f_t
T-SOP [22]	20	235 mA/mm	66 GHz	17.5 GHz
POML	29 V	205 mA/mm	90.5 GHz	18.7 GHz

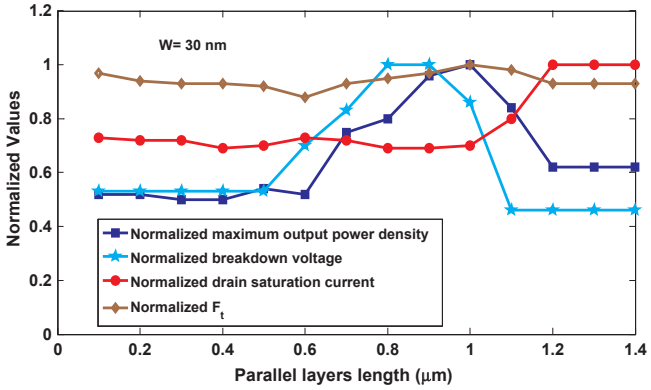

Fig. 12. Optimization of normalized parameters according to the oxide-nickel length at fixed layers width.

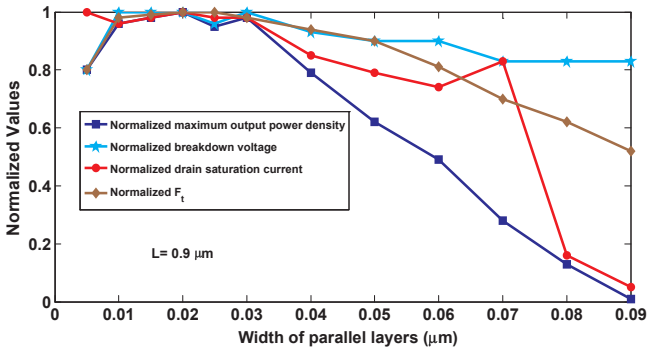

Fig. 13. Optimization of normalized parameters according to the oxide-nickel width where layers length is fixed.

Four important device characteristics have been used as figure of merit for optimizations including breakdown voltage, saturation current, maximum output power density, and cut-off frequency. Wide range simulations reveal that 0.9 μm is the best choice for layer length. Fig. 13

shows optimization results of layers width where their length is fixed at 0.9 μm (obtained from previous figure). It is seen that 30 nano meter is a proper width for layers. It is apparent from Fig. 13 that the width can be selected less than 30 nm but it may create some problems from fabrication point of view. The results from optimization (Fig. 13) and also the obtained RF and DC parameters along the paper reveals that the layers width can be selected wider than 30 nano meter in the conditions that DC and RF performance of the POML remain better than conventional structure (neglecting a trivial reduction in saturation current). This value can be selected even as long as 50 nano meter. This lets to the fabrication process to be done with more efficiency and removes some concerns about process violations from predicted dimensions.

6. Conclusion

In this paper we proposed a novel structure for SOI-MESFETs which includes parallel metal and oxide layers to control the electric field, breakdown voltage and RF characteristics. Using SILVACO-ATLAS simulator we simulated the DC and RF device behaviors. Apart from additional fabrication steps due to added layers which is approximately a common feature for novel structures, main advantages of the proposed structure in comparison with conventional structure are summarized as follows:

- Regarding to the higher critical electric field of oxide region and metal ability in scattering the potential lines in the gate corner, POML structure boosts the breakdown voltage.
- Additional oxide layer operates as a practical blockage in extending the depletion region underneath the gate into the drift region and lowers the coupling between output and input and improves maximum oscillation and cut-off frequencies.
- Metal layer lowers the gate capacitance and causes to more improvement in maximum oscillation and cut-off frequencies.
- Maximum output power density improves due to the higher breakdown voltage.

From these investigations and comparisons, the POML-SOI-MESFET can be regarded as an efficient SOI-MESFET in high speed and high voltage applications.

Appendix A. Supplementary materials

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.aeue.2017.10.025.

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